

BOHAN YANG

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EDUCATION

University of Science and Technology of China (USTC)
School of the Gifted Young (Honor School)

Sept. 2020 – Current
Hefei, China

- GPA: 4.07/4.30 Ranking: 1/34 CGPA: 93.19
- Bachelor of physical electronics
- Interested in **Computer Architecture** and **Digital Chip Design**
- Admitted by Yan Jici Talent Class (Honor Class)
- Class commissary in charge of studies
- English skills:
TOEFL: 105 (R:30 L:26 S:23 W:26) CET-4: 641 CET-6: 587

PUBLICATION

- **Adyna: Accelerating Dynamic Neural Networks with Adaptive Scheduling** (the second author)
[Micro 2023 Under Review, Advisor: Prof. Mingyu Gao]

HONOURS AND AWARDS

National Scholarship (Top 1%)	2021
First Prize of the 13th National College Students Mathematics Contest	2021
Yan Jici Talent Class Scholarship (Top 1%)	2022
Qiangwei Great Ambition Scholarship (Top 1%)	2022
Alumni (Class of 1987) Innovation Scholarship	2023
Qiangwei Dedication Scholarship	2023

RESEARCH EXPERIENCES

Research Intern

IIIS, Tsinghua University

Oct. 2022 – Current
Advisor: Prof. Mingyu Gao

- Explore dataflow optimization methods on the scalable spatial accelerator for dynamic neural networks
- Construct an HW-SW co-design platform cooperatively, from operator graph scheduler to chip-based dynamic tensor dispatcher and near-SRAM-router
- Build a cycle-accurate simulator based on gem5 and Simpy to implement and simulate our dataflow scheme ideas, evaluate the architecture, and perform relatively precise performance estimation

Intern

Polar Bear Tech

Jul. 2022 – Sept. 2022
Advisor: Huanbing Shi

- As a member of the compiling research group, I implemented AI operators like Conv and DT in C++ for the Qiming 940 AI chip (IR -> binary)
- Verify the functional correctness of operators by generating a large number of sampling cases
- Compose generation scripts and explore how to speed up the generation and reduce the occupation of disks (pruning the parameter space) while ensuring sample coverage rate

Research Intern

School of Microelectronics, USTC

Apr. 2022 – Jun. 2022
Advisor: Prof. Yi Kang

- Implement operators on the accelerator platform developed by the research group in C++

- Optimize specific AI applications like H.265 video encoding algorithms on this platform

PROJECTS

Digital chip design practice Sept. 2022 – Feb. 2023
School of Microelectronics, USTC *Advisor: Xuefei Bai*

- Design a SOC in TSMC 180nm process and explore the whole chain from front-end architecture design to back-end layout generation
- Implement three parts of the SOC: 8-bit MIPS CPU, systolic array accelerator, and SRAM controller
- Manage to quickly iterate the design and simulate the circuit to confirm the correctness of both timing and function using Synopsys and Cadence EDAs

Five-stage-pipelined RISC-V CPU design and SOC design Apr. 2022 – Jun. 2022

- Manage to implement the design of a RISC-V SOC in Verilog RTL
- The SOC includes a classic five-stage-pipelined CPU, UART controller, GPIO (switch and LED light) controller, etc
- Write assembly codes and compile them to do some software tasks like serial port communication and LED light array show

TEACHING

Teaching Assistant Sept. 2022 – Feb. 2023
USTC *Lecturer: Xuefei Bai*

- Answer the questions from freshman students in the period of learning C language, prepare daily exercises and participate in experiment design
- Review the submitted homework and cooperate with the lecturer to complete the student assessment task

SKILLS

- C++ / C / Python / Assembly Language (X86 & RISC-V) / Matlab / Gem5 / Verilog / FPGA development / Cadence & Synopsys EDATools / LaTeX / Markdown
- Interests: Go (10 years) / Football (6 years) / Guitar (8 years)
- Languages: Chinese–Mandarin (Native), English (Fluent)

EXTRACURRICULAR PRACTICES

Summer Course Outstanding Student (grade: 95 A+) Peking University, 2022

The fifth team of the USTC Counter-Strike tactics competition (As Captain) USTC, 2021

Team Final Four in USTC Angel Football Cup USTC, 2020